1. **Using a timer clock source of 8 MHz, calculate PSC and ARR values to get a 60 Hz interrupt.**

* A target frequency of 60Hz results in a 16.67ms period; we then divide the 8Mhz clock by 8000 to reduce our timer’s frequency to 1kHz. Counting at 1 kHz gives us 1 ms per timer count, so we need 16.67 counts to reach our target period. **We can achieve our timing scheme by setting the PSC to 7999, the ARR to 1667/100000, and enabling the UEV interrupt in the control registers.**

1. **Look through the Table 13 "STM32F072x8/xB pin definitions" in the chip datasheet and list all pins that can have the timer 3 capture/compare channel 1 alternate function.**

* If the pin is included on the LQFP64 package that we are using, list the alternate function number that you would use to select it.
* PE3, PA6 (22), PC6 (56), PB4 (37)

1. **List your measured value of the timer UEV interrupt period from first experiment.**

* 4.06 Hz

1. **Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 1.**

* The rate increases as the CCR value increased for PWM mode 1. The length increased (delay).

1. **Describe what happened to the measured duty-cycle as the CCRx value increased in PWM mode 2.**

* The rate increased faster, but it still increases. The length itself (delay) got smaller, got compressed.

1. **Include at least one logic analyzer screenshot of a PWM capture.**

A screenshot of a computer

Description automatically generated

1. **What PWM mode is shown in figure 3.6 of the lab manual (PWM mode 1 or 2)?**

* Mode 2